

L Number	Hits	Search Text	DB	Time stamp
3	1111	buried adj bit adj line\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/18 09:53
4	5	protrud\$3 adj bit adj line	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/18 09:54
5	10235	damascene	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/18 09:54
6	5622	dual adj damascene	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/18 09:55
7	12	(buried adj bit adj line\$1) and (dual adj damascene)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/18 09:55
2	23	elevated adj bit adj line\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/18 10:00
1	63	raised adj bit adj line\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/18 10:16
8	44	(buried adj bit adj line\$1) and damascene	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/18 10:16
9	39	((buried adj bit adj line\$1) and damascene) and memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/18 10:16

EAST - (thinsearch15.wsp:1)

FileViewEditToolsWindowHelp

Active

L3: (1111) buried adj bit adj line\$1

L4: (5) protrud\$3 adj bit adj line

L5: (10235) damascene

L6: (5622) dual adj damascene

L7: (12) 3 and 6

L2: (23) elevated adj bit adj line\$1

L1: (63) raised adj bit adj line\$1

L8: (44) 3 and 5

L9: (39) 8 and memory

Failed

(M) ANTI adj line

DBs: USPAT: US PGFUB: EPO: JPO: DERWENT: IBM: TOS

Default operator: OR

8 and memory

Details

Highlight all items exactly

BackHomeImageTextHTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cla	Inventor	S	C	P	I	Image I
23	<input type="checkbox"/>	<input type="checkbox"/>	US 6333240 B1	20011225	62	Method of spacing a capacitor from a contact site	438/396	257/E21.014; 257/E21.019;		Durcan, D. Mark et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6333
24	<input type="checkbox"/>	<input type="checkbox"/>	US 6329682 B1	20011211	13	Capacitor over bit line memory cell and process	257/306	257/906;		Parekh, Kunal R. et al.	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6329
25	<input type="checkbox"/>	<input type="checkbox"/>	US 6329263 B1	20011211	62	Method of forming a container capacitor structure	438/387	257/E21.646; 257/E21.014;		Durcan, D. Mark et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6329
26	<input type="checkbox"/>	<input type="checkbox"/>	US 6281091 B1	20010828	61	Container capacitor structure and method of formation thereof	438/387	257/E21.019; 257/E21.014;		Durcan, D. Mark et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6281
27	<input type="checkbox"/>	<input type="checkbox"/>	US 6274424 B1	20010814	14	Method for forming a capacitor electrode	438/239	257/E21.019; 257/E21.011;		White, Jr., Bruce E. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6274
28	<input type="checkbox"/>	<input type="checkbox"/>	US 6261905 B1	20010717	14	Flash memory structure with stacking gate formed using damascene-like str	438/264	257/E21.682; 257/E27.103;		Chen, Jong et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6261
29	<input type="checkbox"/>	<input type="checkbox"/>	US 6204127 B1	20010320	6	Method of manufacturing bit lines in memory	438/270	257/E21.671		Wang, Ling-Sung	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6204
30	<input type="checkbox"/>	<input type="checkbox"/>	US 6180452 B1	20010130	22	Shared length cell for improved capacitance	438/255	257/E21.012; 257/E21.019;		Figura, Thomas A.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6180
31	<input type="checkbox"/>	<input type="checkbox"/>	US 6172387 B1	20010109	19	Semiconductor interconnection structure and method	257/296	257/306;		Thakur, Randhir P. S. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6172
32	<input type="checkbox"/>	<input type="checkbox"/>	US 6168985 B1	20010102	62	Semiconductor integrated circuit device including a DRAM having red	438/241	257/E21.011; 257/E21.646;		Asano, Isamu et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6168
33	<input type="checkbox"/>	<input type="checkbox"/>	US 6159818 A	20001212	61	Method of forming a container capacitor structure	438/387	257/E21.648; 257/E21.019;		Durcan, D. Mark et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6159
34	<input type="checkbox"/>	<input type="checkbox"/>	US 6130102 A	20001010	13	Method for forming semiconductor device including a dual inlaid structur	438/3	257/E21.658; 257/E21.011;		White, Jr., Bruce E. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6130
35	<input type="checkbox"/>	<input type="checkbox"/>	US 6060351 A	20000509	14	Process for forming capacitor over bit line memory cell	438/253	257/E21.648; 257/E21.646;		Parekh, Kunal R. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6060
36	<input type="checkbox"/>	<input type="checkbox"/>	US 6037207 A	20000314	62	Method of manufacturing semiconductor integrated circuit devi	438/241	257/E21.648; 257/E21.646;		Asano, Isamu et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6037
37	<input type="checkbox"/>	<input type="checkbox"/>	US 6025624 A	20000215	21	Shared length cell for improved capacitance	257/306	257/307; 257/309;		Figura, Thomas A.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6025
38	<input type="checkbox"/>	<input type="checkbox"/>	US 5858833 A	19990112	14	Methods for manufacturing integrated circuit memory devices including tren	438/253	257/E21.648; 257/E27.086;		Lee, Won-seong et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 5858
39	<input type="checkbox"/>	<input type="checkbox"/>	US 6403424 B	20020611	13	Formation of self-aligned mask read only memory by forming dual damas				CHUNG, H et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 6403

Ready

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